

REMARKS/ARGUMENTS

Applicant acknowledges the rejection of Claims 1-20 and 22-24 with a right to traverse. Claims 1-6, 7-15, 18-20, and 22 are currently amended; Claims 23 and 24 are canceled; and Claims 25 and 26 are newly added. As a result, Claims 1-20, 22, 25, and 26 are pending in this application. No new matter has been introduced.

Applicant respectfully requests further examination and reconsideration of the rejections for the reasons stated below.

Claim Objections

Claims 23 and 24 are objected because of informalities. Claims 23 and 24 are canceled herein therefore, the objections are moot.

§103 Rejection of the Claims

Claims 1-3 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over U.S. Patent No. 6,553,472 (hereinafter "Yang") in view of U.S. Patent No. 6,606,041 (hereinafter "Johnson").

Applicant respectfully submits that the rejection fails to establish a *prima facie* case of obviousness since the combined references of Yang and Johnson fail to teach each and every element of the Claims.

Currently amended independent Claim 1 is recited below:

1. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:
 - generating command signals to access an integrated circuit component;
 - accessing data signals to convey data for the integrated circuit component;
 - accessing sampling signals to control sampling of the data signals; and
 - systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device.

The rejection states that Yang does not disclose "automatically adjusting a phase (timing) between the command signals, the data signals, and the clock (sampling) signals to calibrate (optimize) operation of the integrated circuit device," but alleges that Johnson "discloses calibrating timing (phase) relationship between control (command) and data signals (see section 0001), wherein calibrating the timing relationship between the data and command blocks also correctly calibrates the sampling (signals) of the data (see section 0006)" as recited in previously presented Claim 1.

However, regarding amended Claim 1, Applicant respectfully submits that the combined references fail to teach or suggest the claimed limitations of "systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device." Although section 0001 of Johnson teaches calibrating the timing of control and data signals in DRAM memory devices, Johnson fails to teach or suggest calibrating timing of sampling of the data signals. In addition, even though section 0006 of Johnson recites sampling of data by synchronously timing command clock signals and data clock signals, Johnson fails to teach or suggest the claimed limitations of systematically altering respective phase shifts of the command, data, and sampling signals to determine a valid operation range of the integrated device. That is, Johnson discloses achieving sampling or timing calibration by determining an optimal delay for the command signals and the data signals, whereas Claim 1 recites the determination of the valid range of the integrated circuit device by systematically altering the phase shift of the sampling signals as well as the phase shift of the command signal and the phase shift of the data signal, as claimed. Since the combined references fail to teach each and every element of Claim 1, Applicant respectfully requests the withdrawal of the rejection, and solicits allowance of Claim 1. Since Claims 2 and 3 are dependent on allowable Claim 1, the Claims overcome the rejections of record by virtue of their dependency to Claim 1 and for the additional features they recite, and respectfully solicit allowance of these Claims.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, and further in view of U.S. Patent No. 6,850,459 (hereinafter "Suzuki"). Since Claims 4-6 are dependent on allowable Claim 1, the Claims overcome the rejections of record by virtue of their dependency to Claim 1 and for the additional features they recite. Accordingly, Applicant respectfully solicits allowance of these Claims.

Claims 7, 8, 12, and 22 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, and further in view of U.S. Patent No. 6,898,683 (hereinafter "Nakamura"). Since independent Claims 7, 12, and 22 recite at least those features similar to that of Claim 1, and they are therefore patentable over the cited references for the same reasons. As such, allowance of the Claims is earnestly solicited. Since Claim 8 is dependent on allowable Claim 7, the Claim overcomes the rejection of record by virtue of its dependency to Claim 7 and for the additional features it recites. Accordingly, Applicant respectfully solicits allowance of the Claim.

Claims 9-11 and 15-18 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, further in view of Nakamura, and yet further in view of Suzuki. Since Claims 9-11 are dependent on allowable Claim 7, the Claims overcome the rejection of record by virtue of their dependency to Claim 7 and for the additional features they recite. Accordingly, Applicant respectfully solicits allowance of

the Claims. Likewise, since Claims 15-17 overcome the rejection of record by virtue of their dependency to Claim 12 and for the additional features they recite, they should be allowed accordingly. Independent Claim 18 recites at least those features similar to that of Claim 1 and is therefore patentable over the cited references for the same reasons.

Claims 13, 14, 23, and 24 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, further in view of Nakamura, and yet further in view of U.S. Patent Application 6,016,282 (hereinafter "Keeth"). Since Claims 13 and 14 are dependent on Claim 12, the Claims overcome the rejection of record by virtue of their dependency to Claim 12 and for the additional features they recite, and respectfully solicit allowance of the Claims. Likewise, Claims 23 and 24 should be allowed for their dependency to Claim 22 and for the additional features they recite, and the Applicant respectfully solicits allowance of the Claims.

Particularly, regarding previously presented Claim 13, the rejection states that the combined references of Yang, Johnson, Nakamura, and Keeth teach the claimed limitations as Keeth "states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, lines 46-55)." However, Applicant respectfully asserts that the combined references fail to teach or suggest the claimed limitations of "performing a coarse calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step

interval to determine if the valid operating range of the DRAM component exists, and if the valid operating range exists, then performing a fine calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal operating mode of the DRAM component.”

Applicant respectfully submits that Keeth fails to disclose that the coarse calibration performed by the vernier clock adjustment circuit determines “if the valid operating range of the DRAM component exists,” as claimed. Unlike Claim 13, Keeth discloses that the coarse calibration performed by the vernier clock adjustment circuit provides coarse steps defined in bit periods (see column 4, lines 15-18). Furthermore, Applicant respectfully asserts that Keeth fails to teach or suggest that the fine calibration performed by the vernier clock adjustment circuit is used to “identify an optimal operating mode of the DRAM component,” as claimed. Instead, unlike Claim 13, Keeth discloses that the fine calibration performed by the vernier clock adjustment circuit provides fine steps to cover adjustments within a single bit period (see column 4, lines 15-18). Since the combined references fail to teach each and every element of Claim 13, Applicant respectfully requests the withdrawal of the rejection and solicits allowance of Claim 13.

Accordingly, allowance of the pending Claims 1-20, 22, 25, and 26 is earnestly solicited.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/716,320

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Title: A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

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Conclusion

Applicant respectfully submits that the Claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

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